Exhibit 20

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification

DDR4 SDRAM Load Reduced DIMM Design Specification

Revision 1.00

August 2015

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

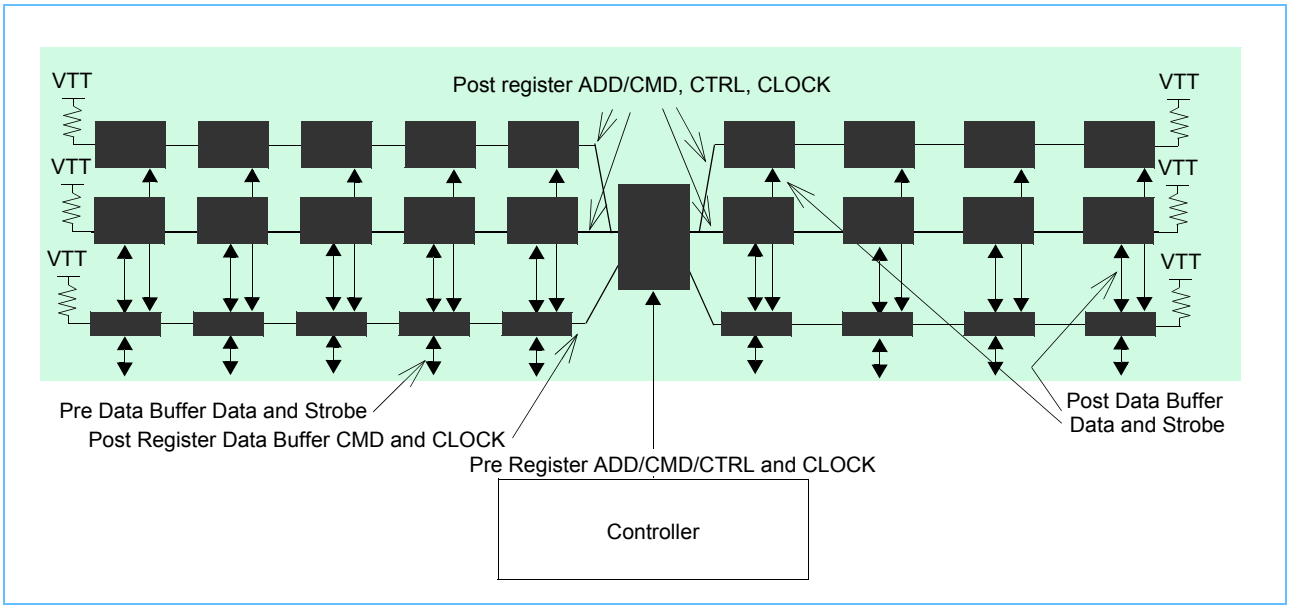

Figure 3 — LRDIMM Topologies

6.2 General Net Structure Routing Rules

The usual design process should be followed to develop an adequate design. Simulations are typically required and timing budgets considered to verify adequate performance. Documenting line lengths alone